What is claimed is:

1. A data processing apparatus configured to perform a pipeline processing in a plurality of divided stages, comprising:

a first pipeline processing portion configured to perform the processing in each stage based on a control signal inputted to each stage;

a first latch portion configured to latch said control signal inputted to each stage with a predetermined clock; and

a second pipeline processing portion, disposed separately from said first pipeline processing portion, configured to perform the processing in each stage based on the control signal latched by said first latch portion.

2. The data processing apparatus according to claim 1, wherein said control signal is a signal for controlling whether or not the pipeline processing is stalled.

3. The data processing apparatus according to claim 1, further comprising second latch portion configured to latch a processing result in at least one stage in said first pipeline processing portion with said predetermined clock,

wherein said second pipeline processing portion utilizes data latched by said second latch portion to perform the processing in the stage corresponding to the data latched by said second latch portion.

4. The data processing apparatus according to claim 1, further comprising:

a third latch portion configured to latch a processing result in at least one stage in said second pipeline processing portion with said predetermined clock; and

a selector configured to select either one of data before latched by said third latch portion and data latched by said third latch portion,

wherein said selector selects a latch output of said third latch portion after the completion of stall and transmits the

latch output to said first pipeline processing portion, if said first pipeline processing portion is stalled when the processing result in said second pipeline processing portion is transmitted to said first pipeline processing portion, and selects the processing result in said second pipeline processing portion and transmits the processing result to said first pipeline processing portion, when said first pipeline processing portion is not stalled.

5. The data processing apparatus according to claim 1, wherein said latch portion latches said control signal with a clock for dividing the respective stages.

6. The data processing apparatus according to claim 1, wherein said second pipeline processing portion performs the pipeline processing later by one cycle or more of a clock for dividing the stages of said first pipeline processing portion.

7. The data processing apparatus according to claim 1, wherein said second pipeline processing portion performs the pipeline processing later by less than one cycle of a clock for dividing the stages of said first pipeline processing portion.

8. The data processing apparatus according to claim 1, wherein one of said first and second pipeline processing portions includes an integer operation unit, and the other includes an operation unit other than the integer operation unit, and

one of said first and second pipeline processing portions includes at least one of a load/store operation unit and a branch operation unit, or includes neither the load/store operation unit nor the branch operation unit.

9. A data processing method for performing first and second pipeline processings by dividing in a plurality of stages, comprising steps of:

performing said first pipeline processing for each stage based on a control signal inputted to each stage;

performing a first latch processing to latch said control signal inputted to each stage with a predetermined clock; and

performing a second pipeline processing for each stage based on said latched control signal separately from said first pipeline processing.

10. The data processing method according to claim 9, wherein said control signal is a signal for controlling whether or not the pipeline processing is stalled.

11. The data processing method according to claim 9, further comprising a step of performing a second latch processing to latch a processing result in at least one stage in said first pipeline processing with said predetermined clock,

wherein said second pipeline processing comprises a step of utilizing data latched by said second latch processing , when performing the processing in the stage for the data latched by said second latch processing.

12. The data processing method according to claim 9, further comprising steps of:

performing a third latch processing to latch a processing result in at least one stage in said second pipeline processing with said predetermined clock; and

selecting either one of data before latched by said third latch processing and data latched by said third latch processing,

wherein said selecting step includes steps of: selecting a latch output of said third latch processing after the completion of stall and transmitting the latch output to said first pipeline processing, when the processing result in said second pipeline processing is transmitted to said first pipeline processing and said first pipeline processing is stalled; and selecting the processing result in said second pipeline processing and transmitting the processing result to said first pipeline processing, when said first pipeline processing is not stalled.

13. The data processing method according to claim 9, wherein

said first latch processing comprises a step of latching said control signal with a clock for dividing the respective stages.

14. The data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing later by one cycle or more of a clock for dividing the stages of said first pipeline processing.

15. The data processing method according to claim 9, wherein said second pipeline processing performs the pipeline processing later by less than one cycle of a clock for dividing the stages of said first pipeline processing.